

Figure 1  
(Prior Art)

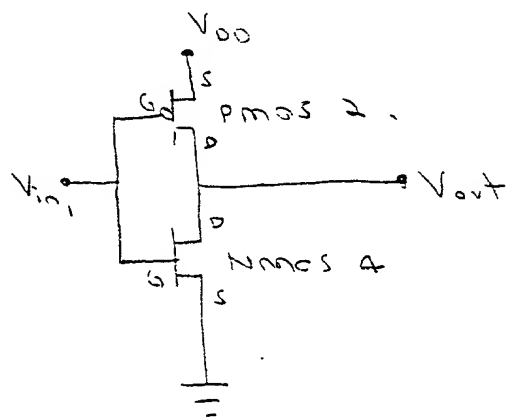


Figure 2  
(Prior Art.)

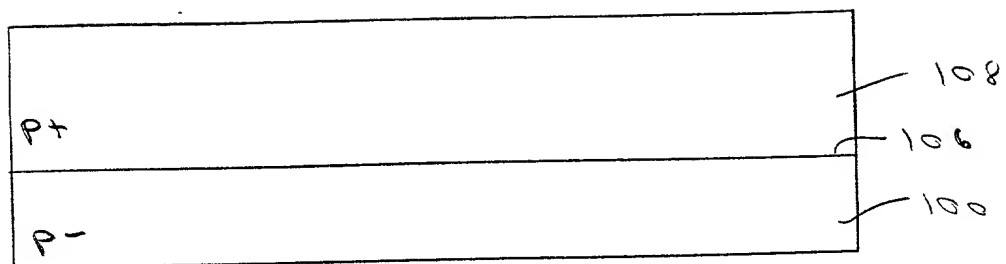


Figure 3

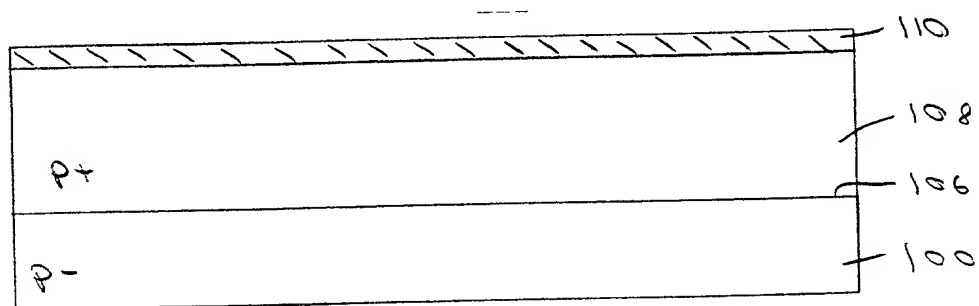


Figure 4

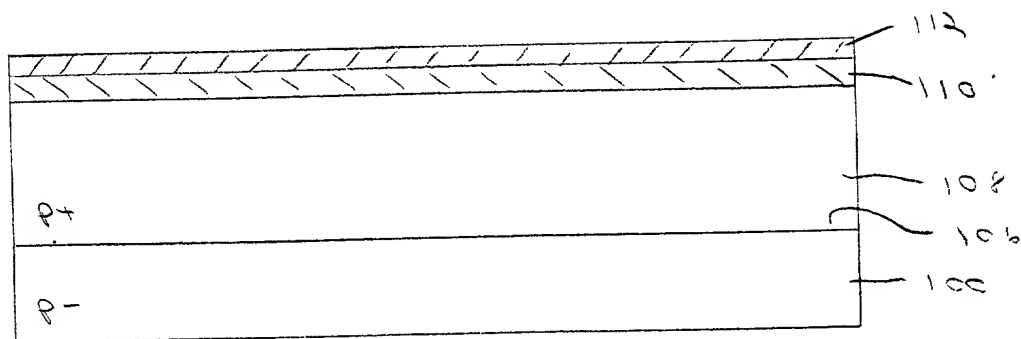


Figure 5

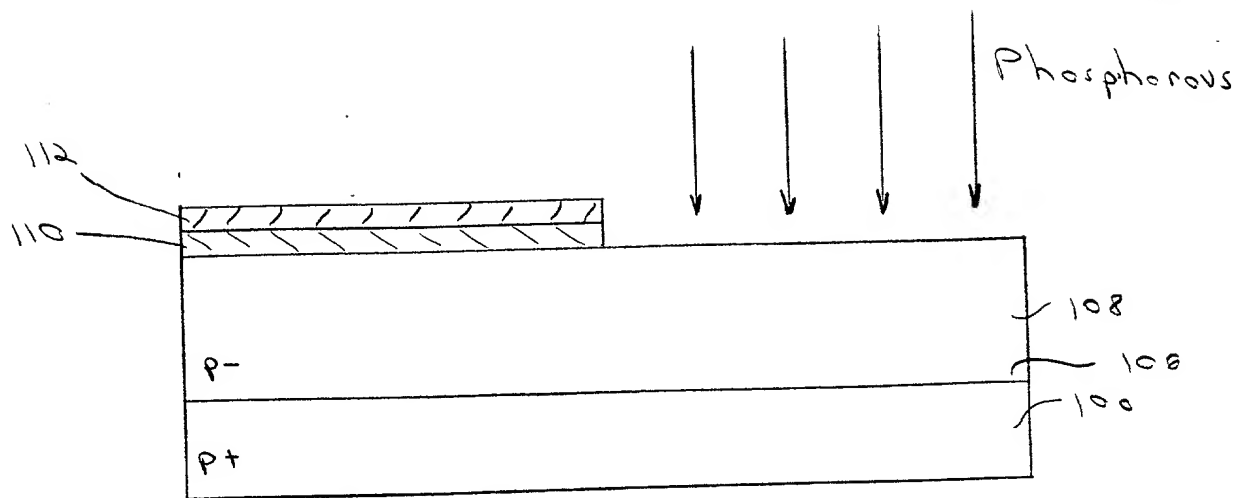


Figure 6

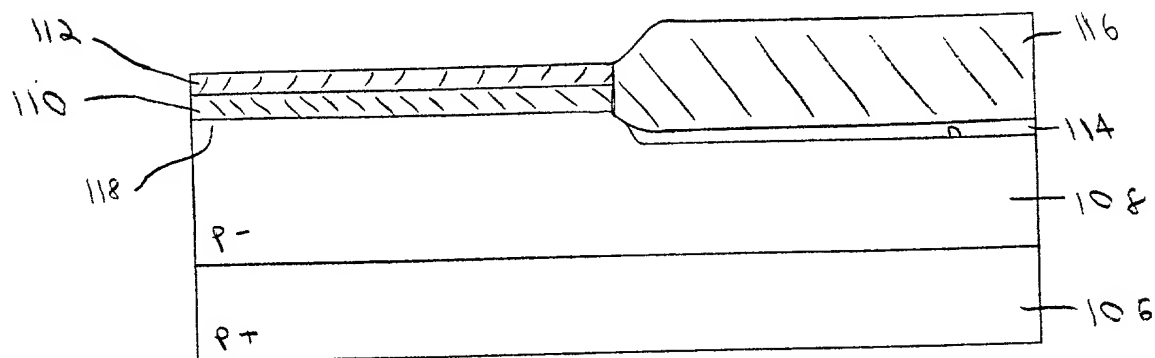


Figure 7

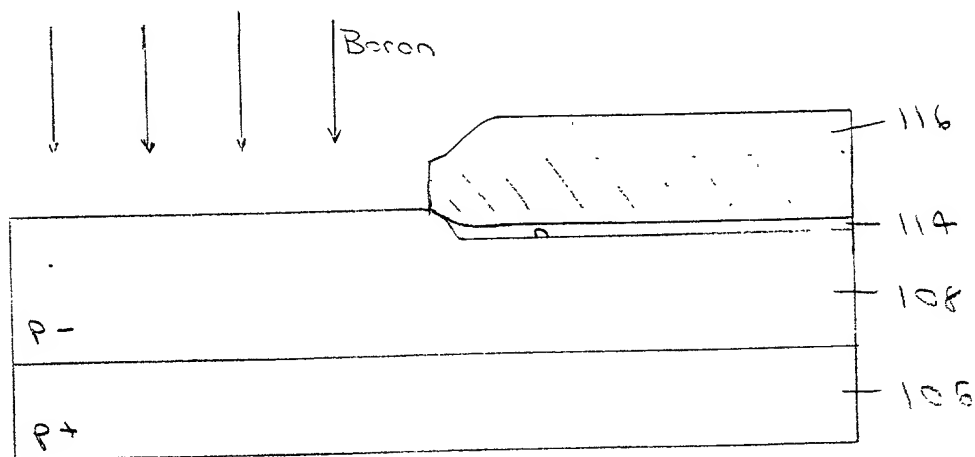


Figure 8

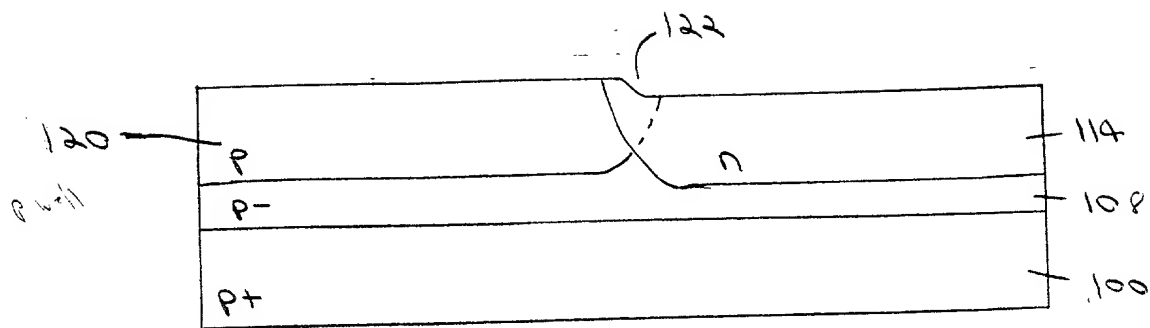


Figure 9

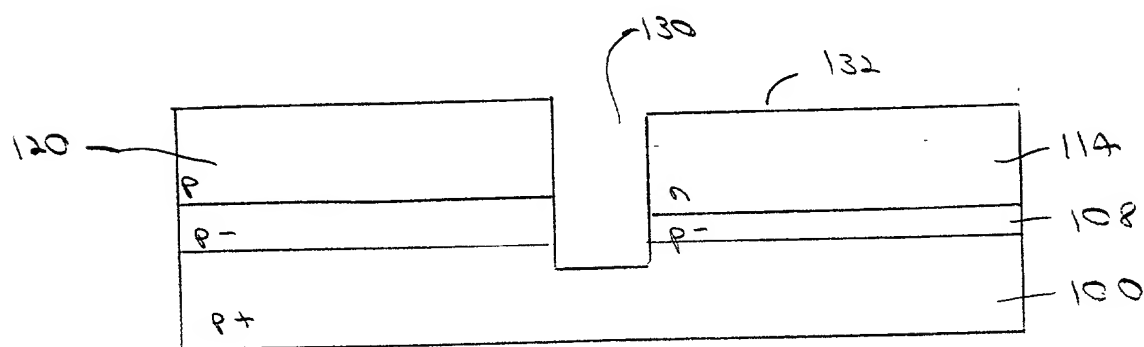


Figure 10

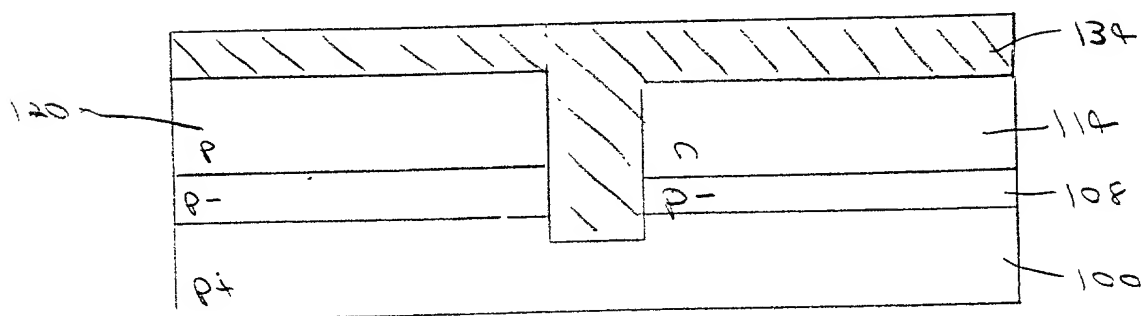


Figure 11

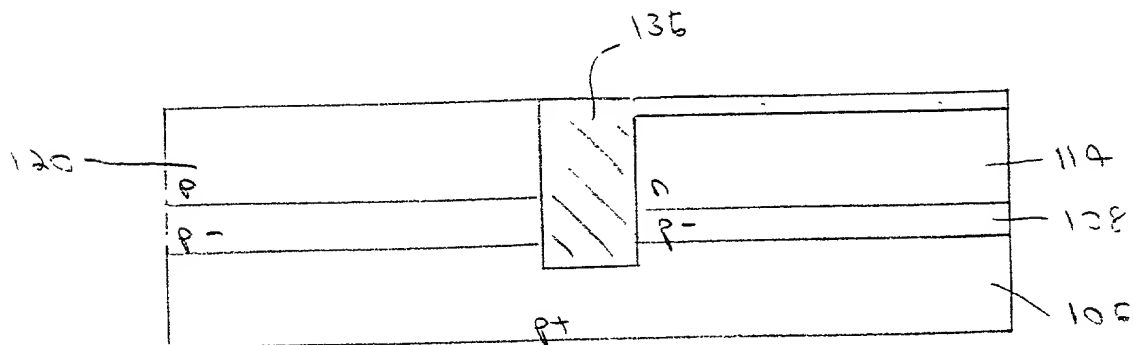


Figure 12

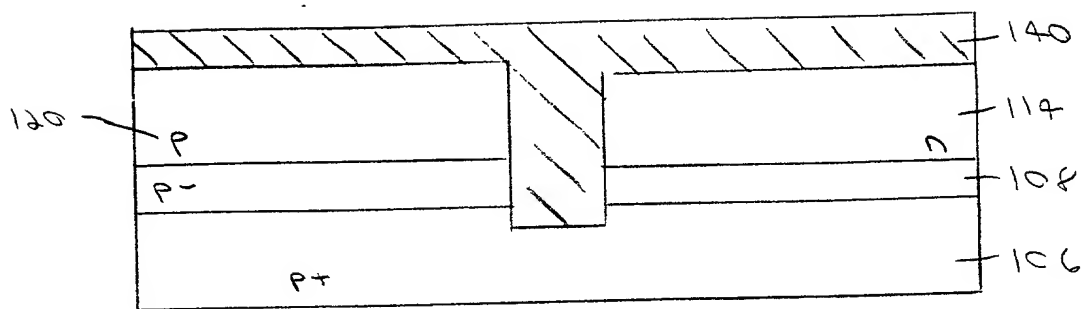


Figure 13

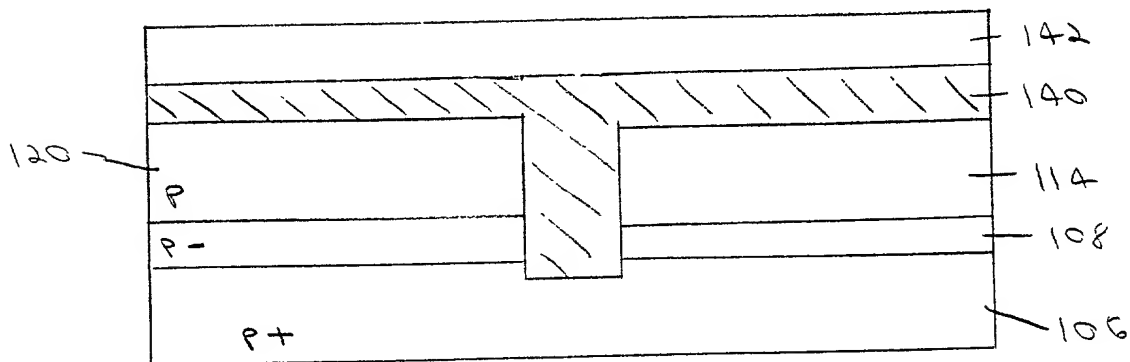


Figure 14

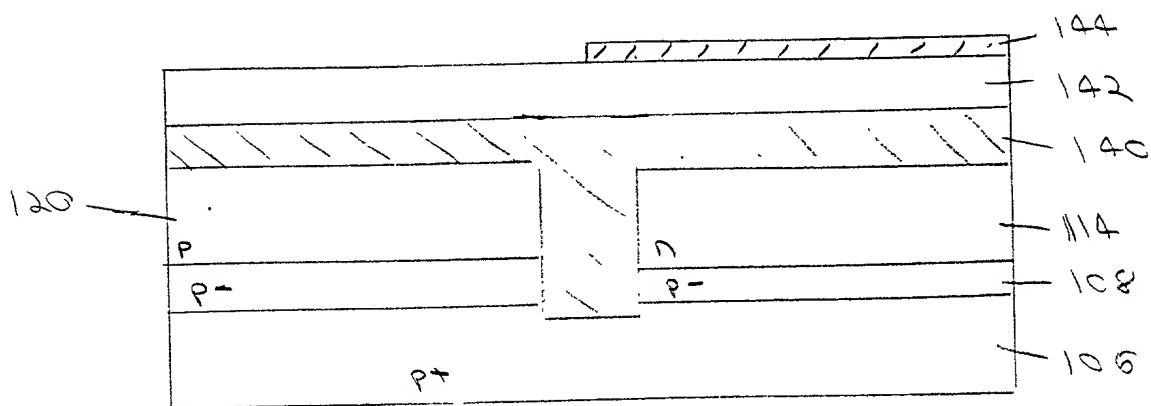


Figure 15

A cross-sectional view of a semiconductor device. A central raised region is formed on a substrate 106. This region contains a stack of layers: a bottom layer 108, a middle layer 114, and a top layer 140. Above layer 140 is a thin layer 142, followed by a layer 144 with diagonal hatching, and a topmost layer 146. The central region is flanked by two side regions. The left side region consists of layers 120, P, P-, and P+. The right side region consists of layers P-, P, and P+. A dashed line is shown within the top layer 140 of the central region.

[illegible]

Figure 18

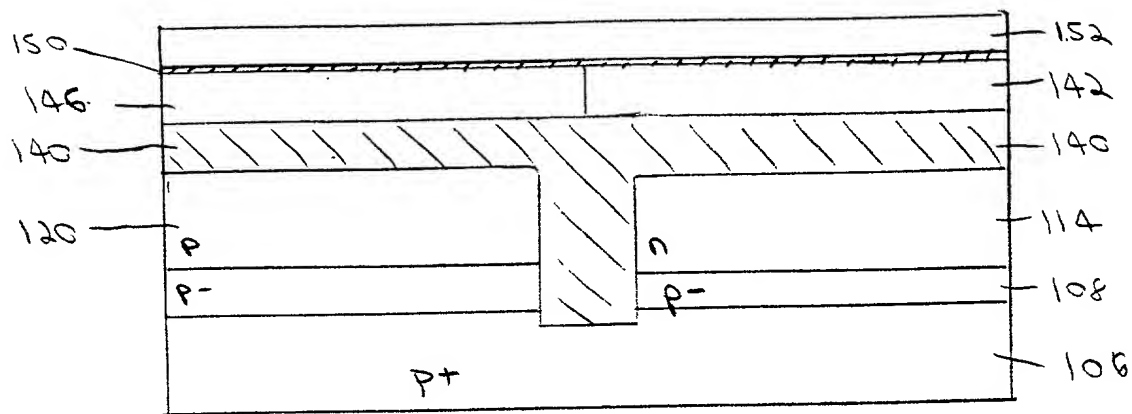


Figure 19

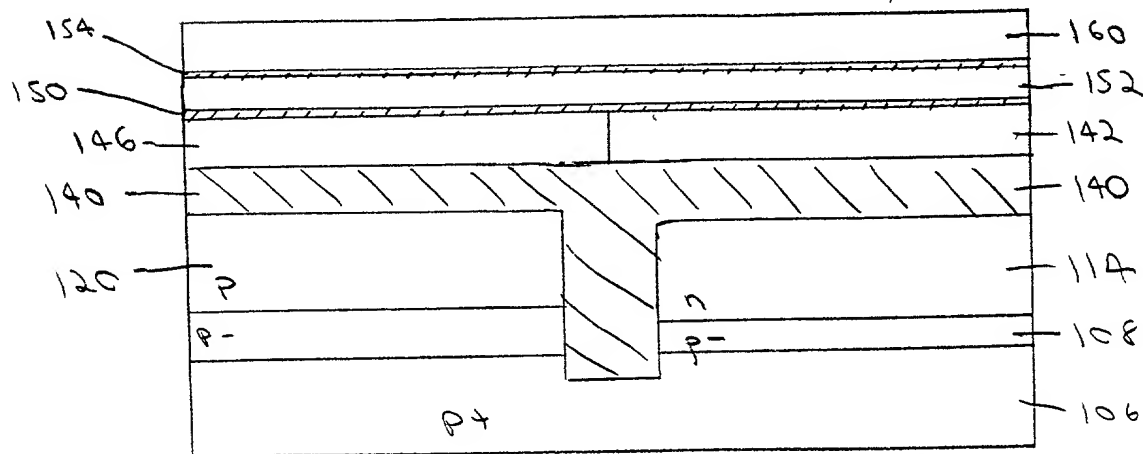


Figure 20

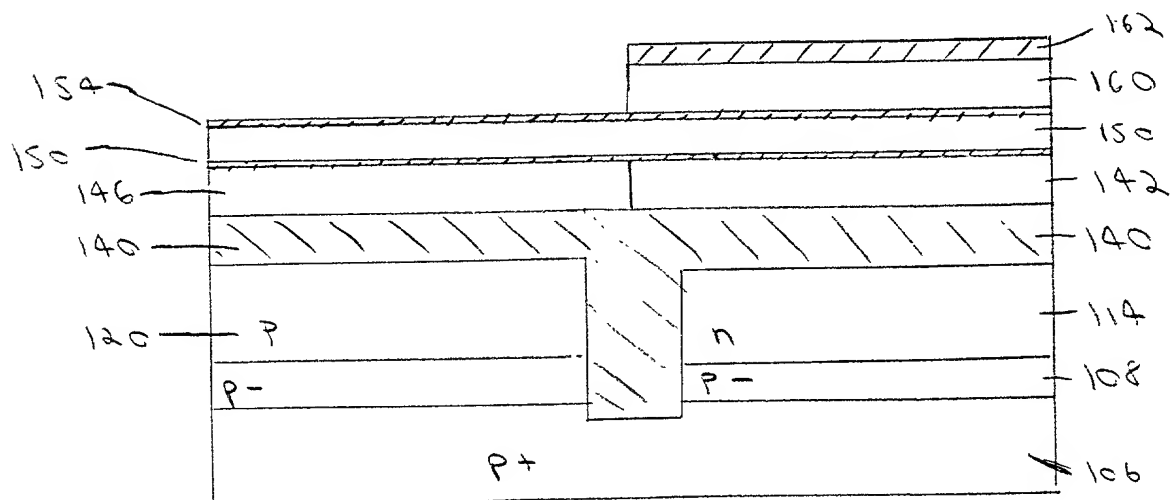


Figure 21

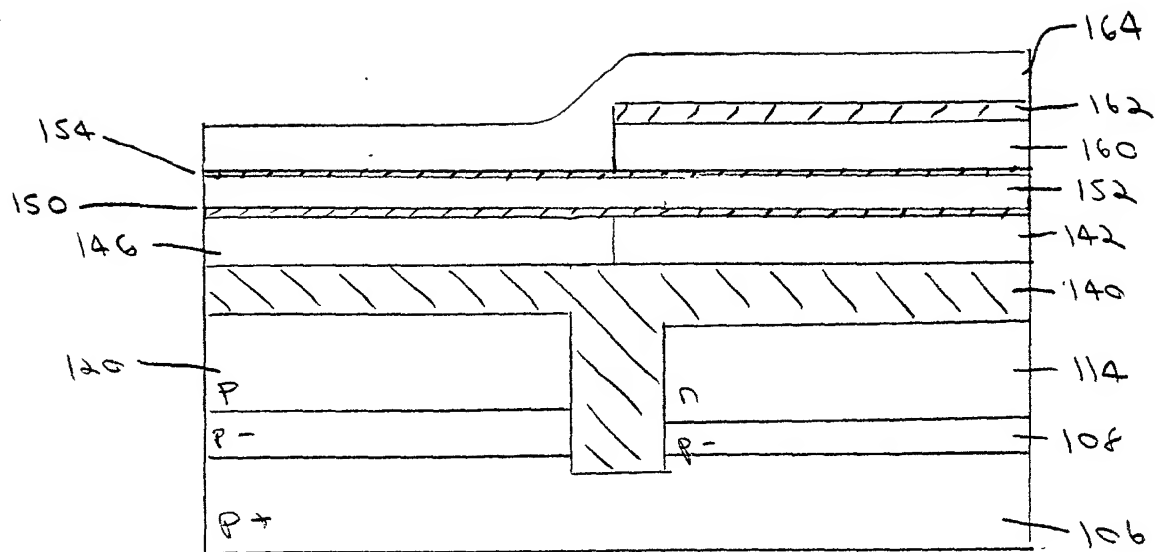


Figure 22

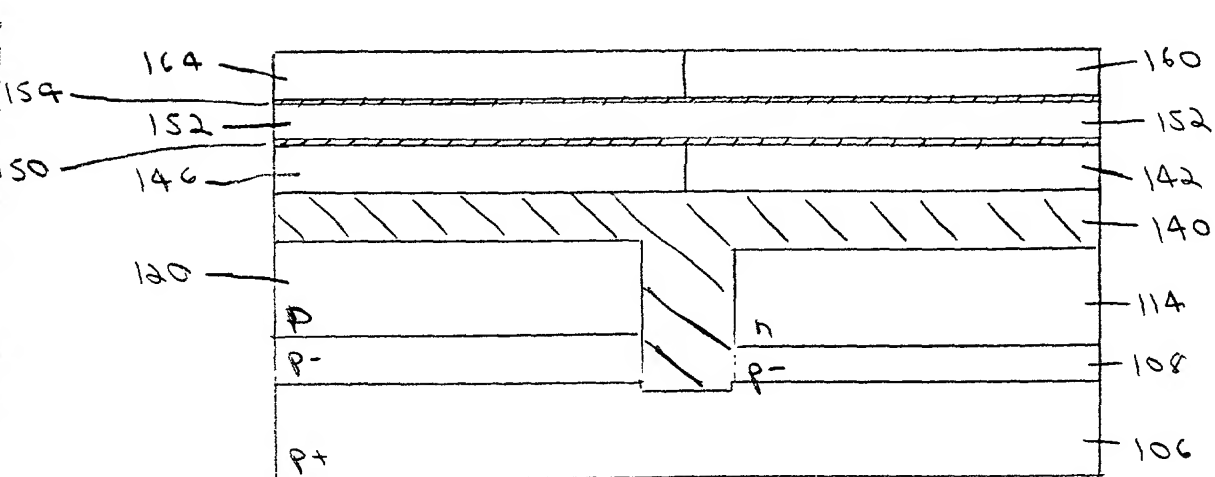


Figure 23

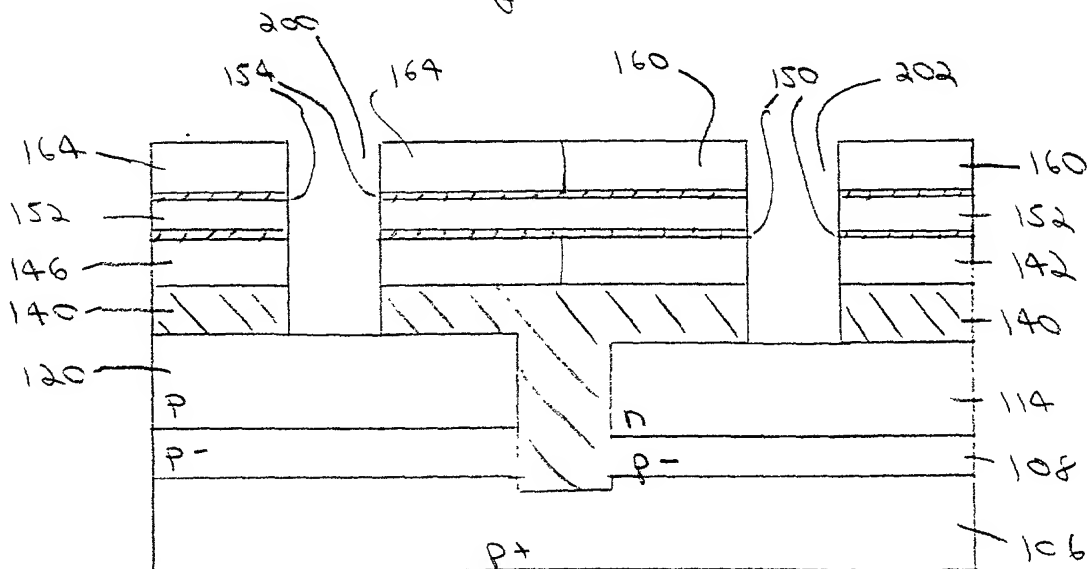


Figure 24



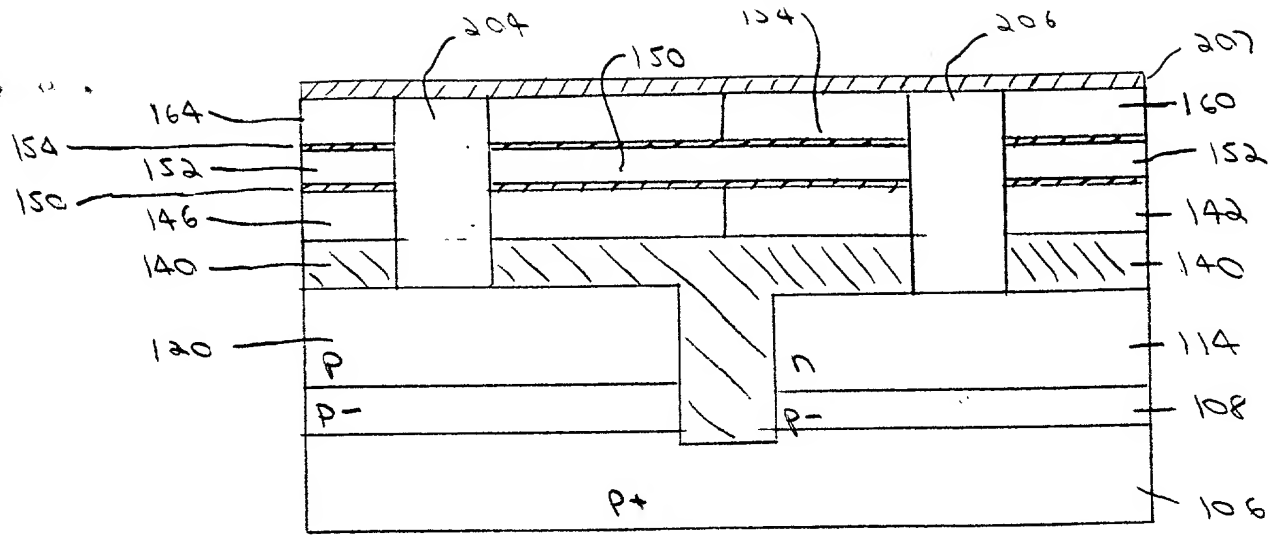


Figure 25

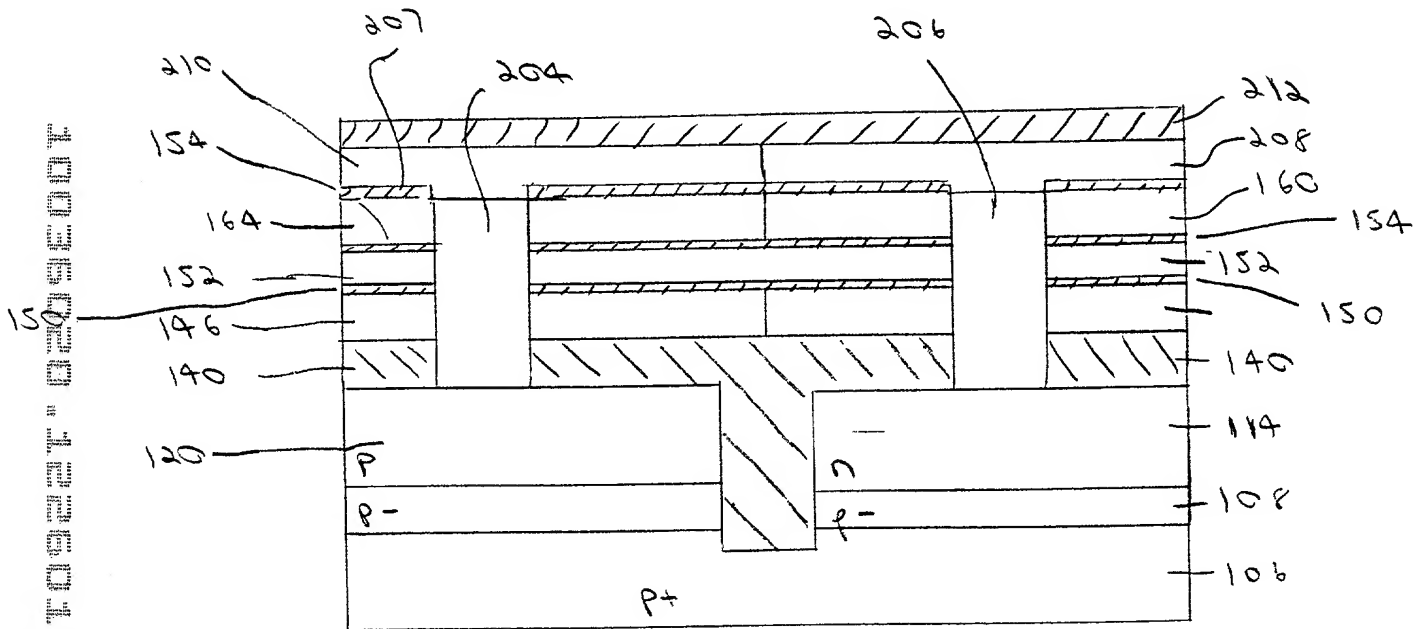


Figure 26

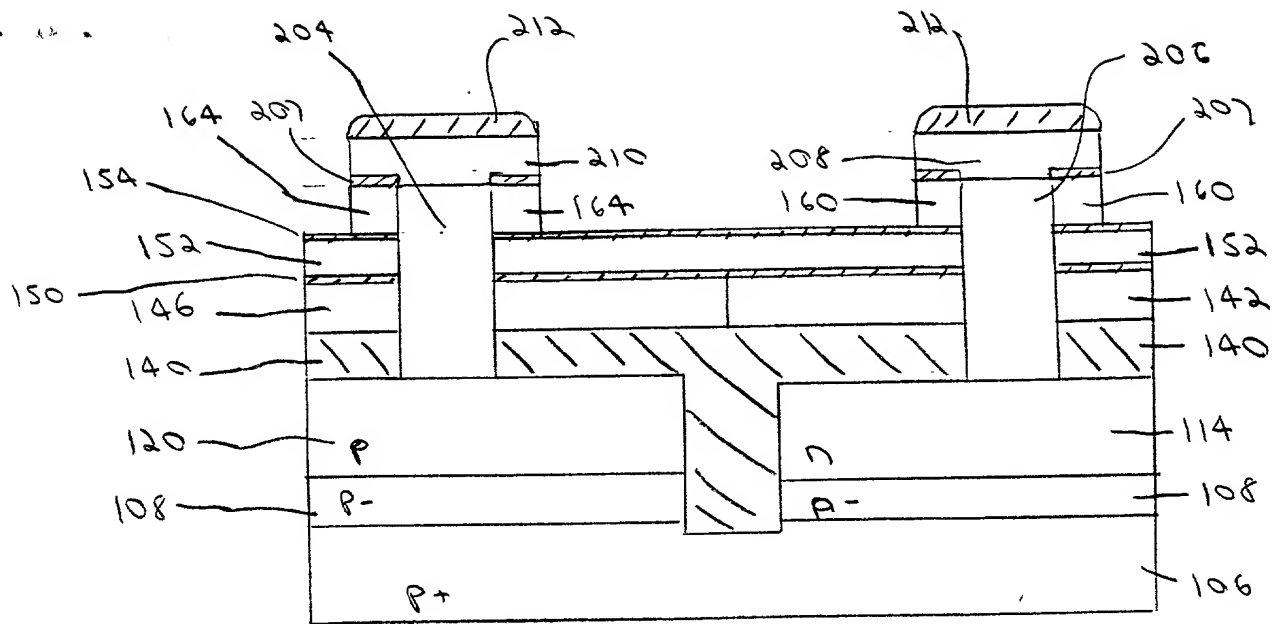


Figure 27

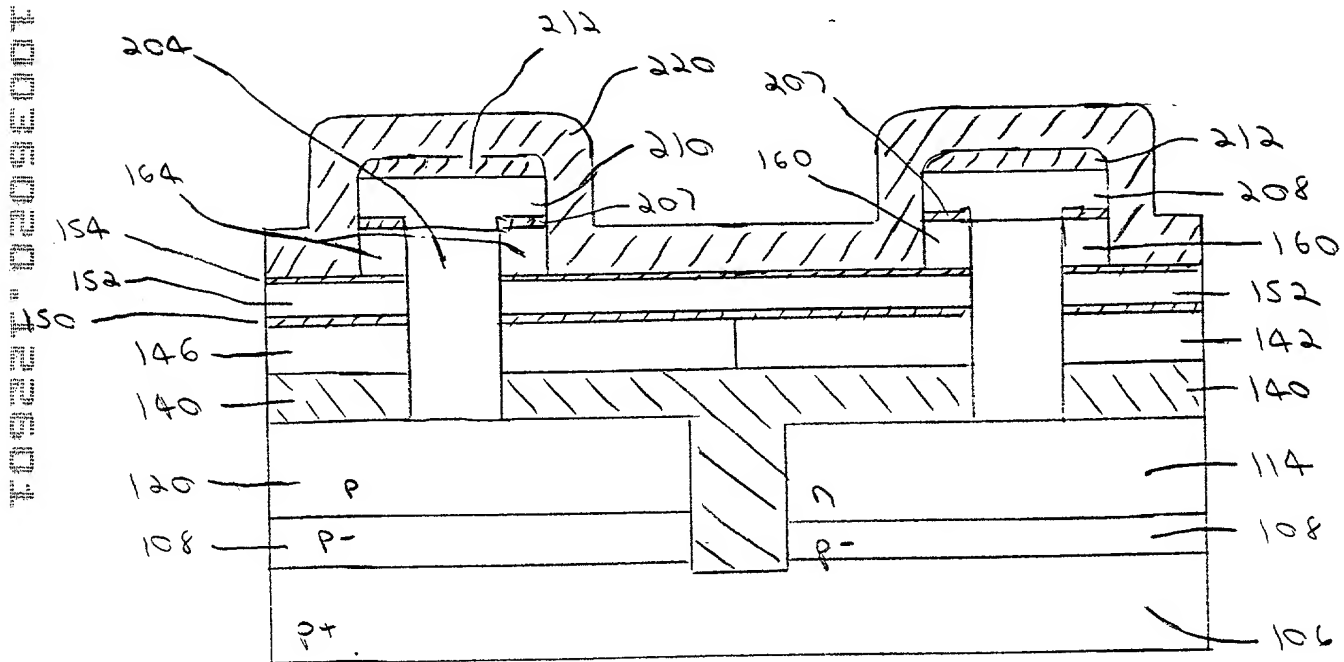


Figure 28

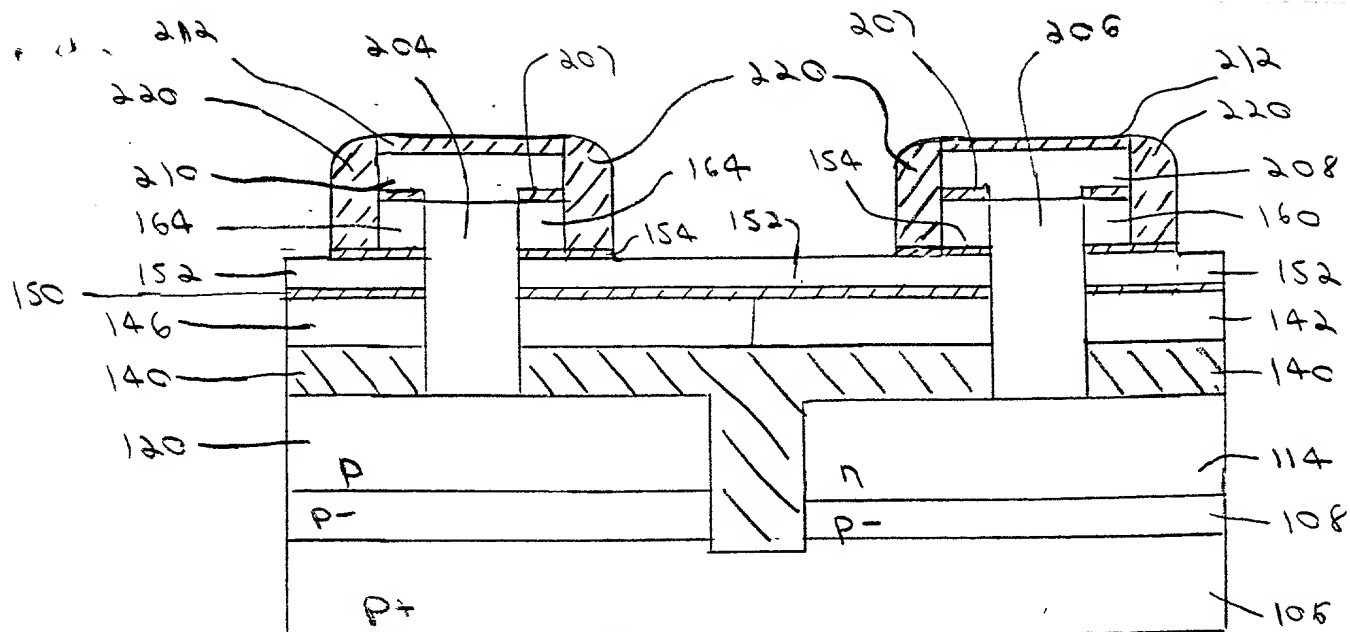


Figure 29

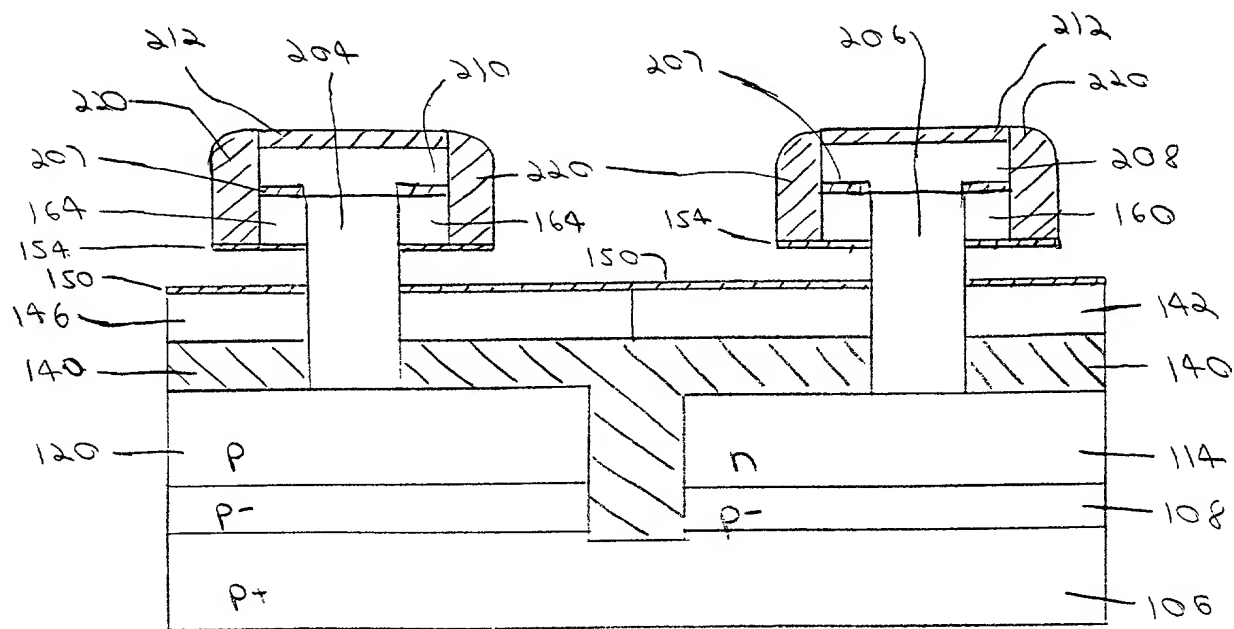


Figure 30

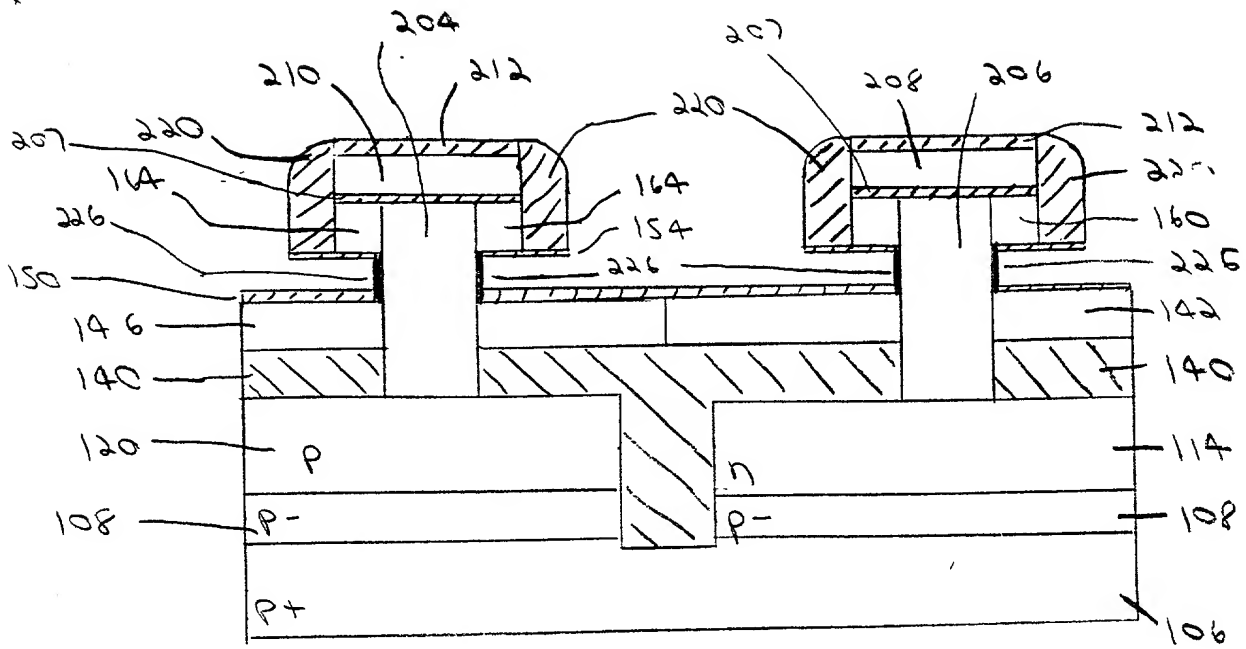


Figure 31

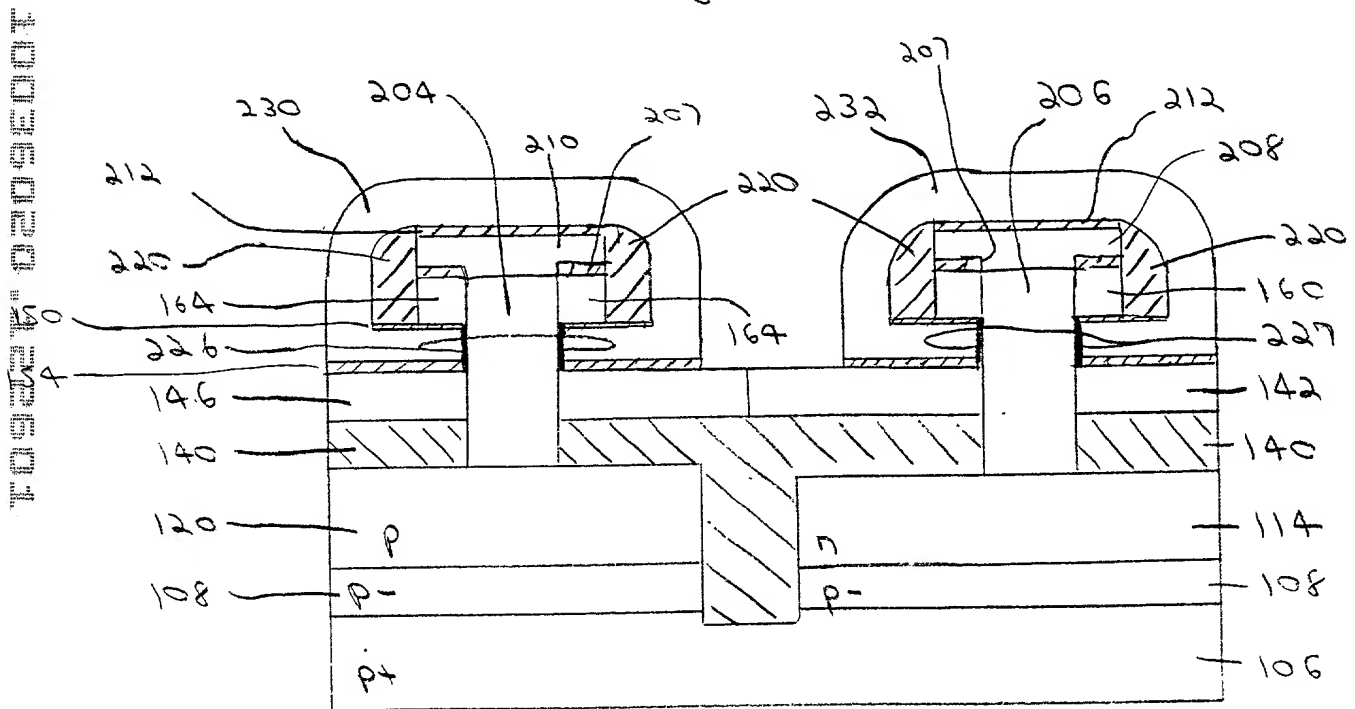


Figure 32

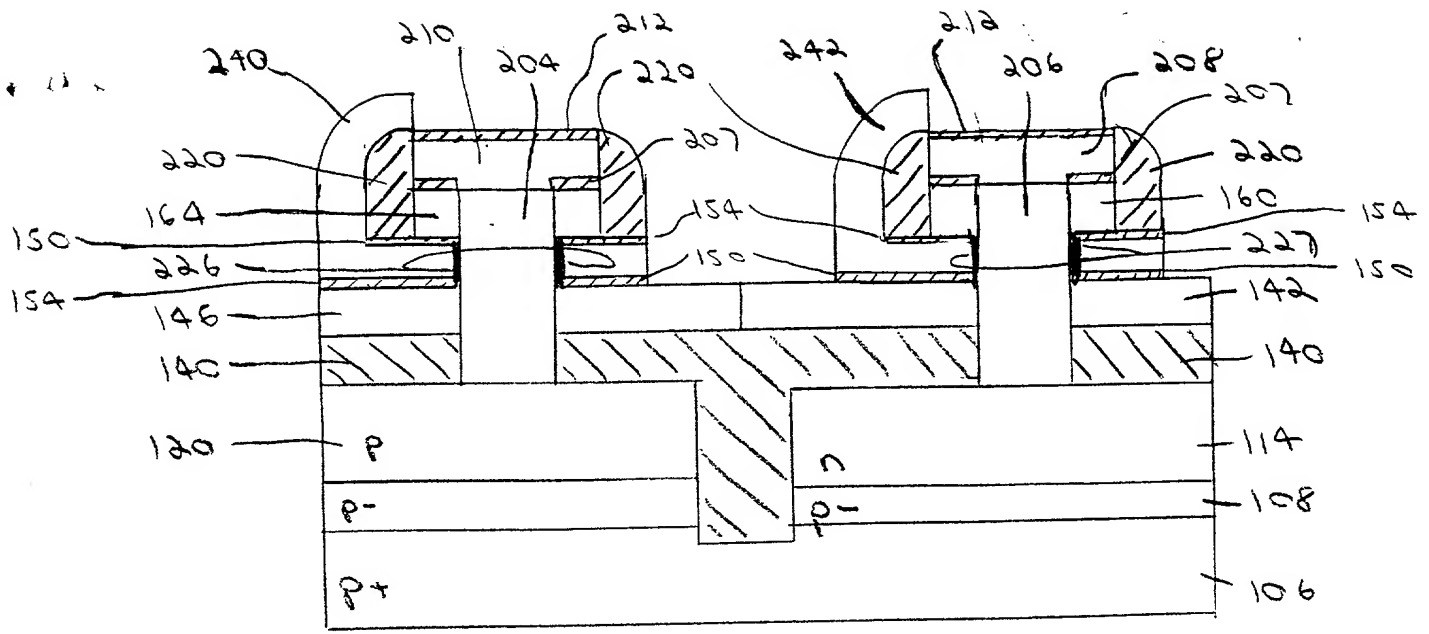


Figure 33

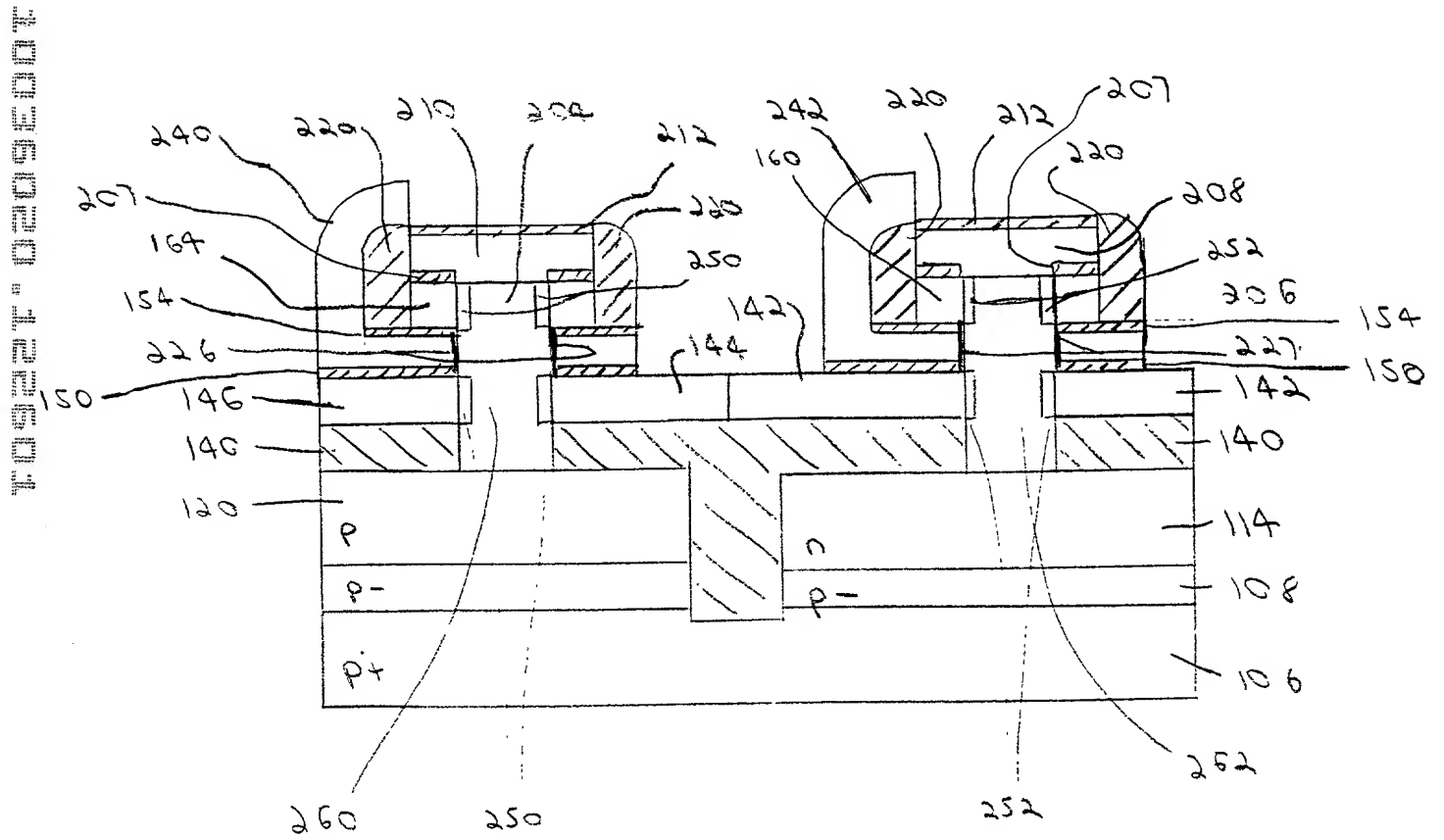


Figure 34

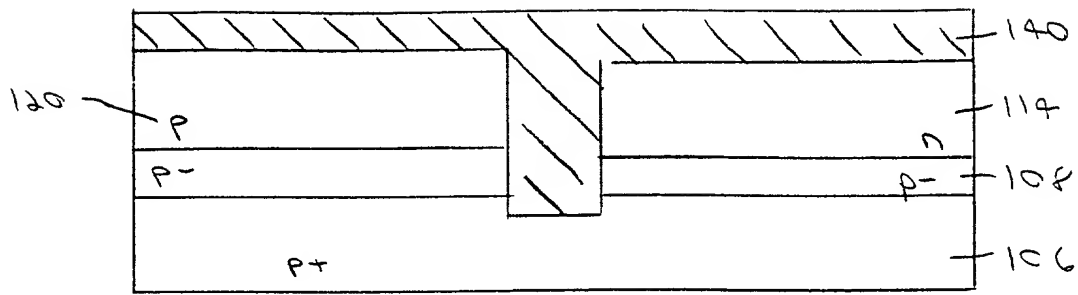


Figure 35

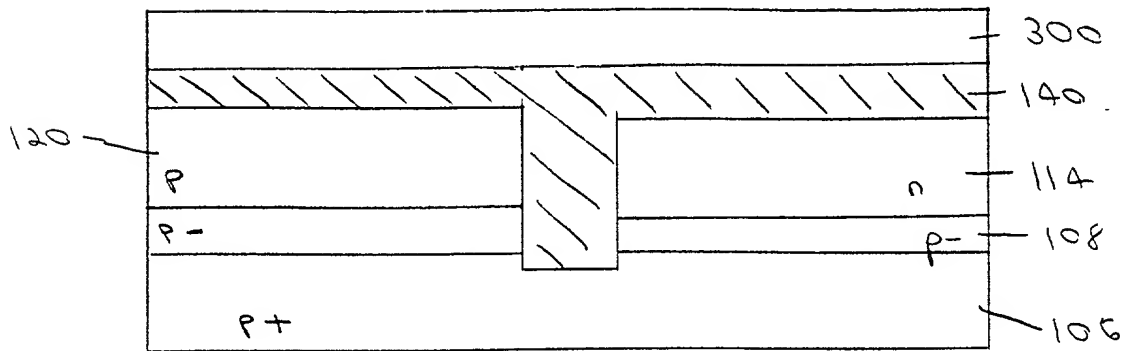


Figure 36

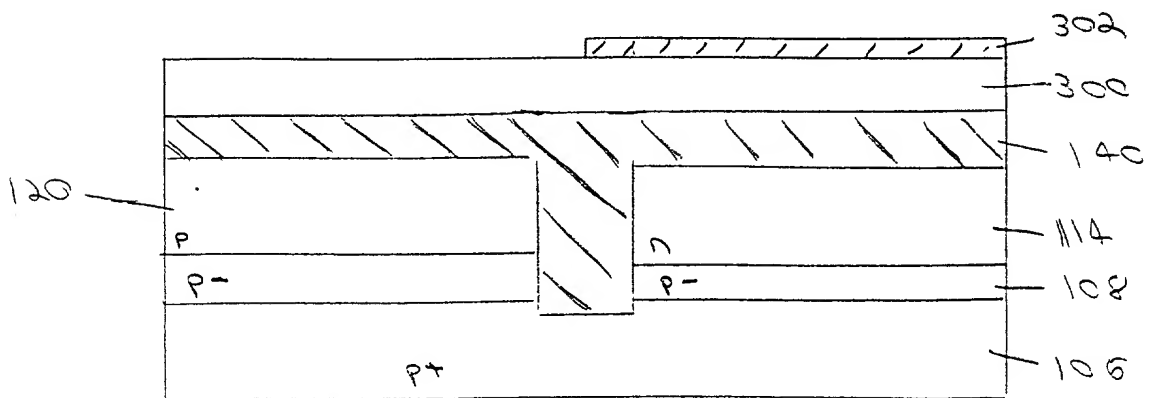


Figure 37

10036030.12504

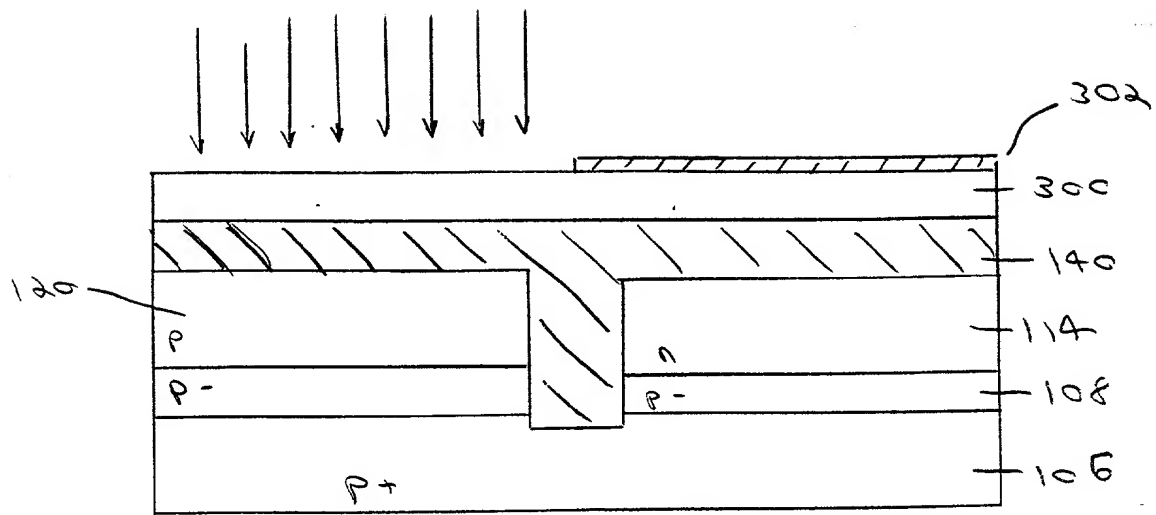


Figure 38

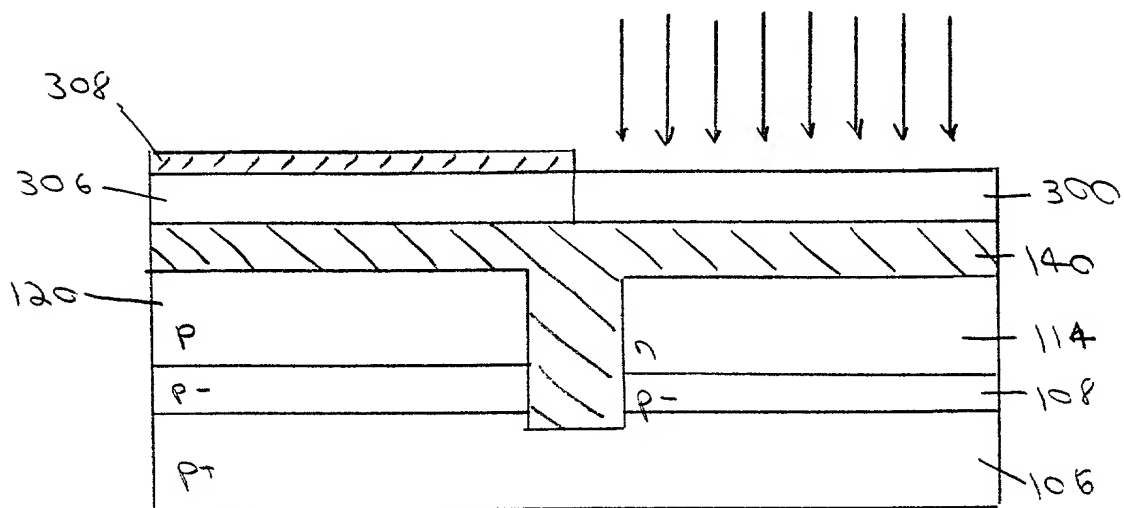


Figure 39

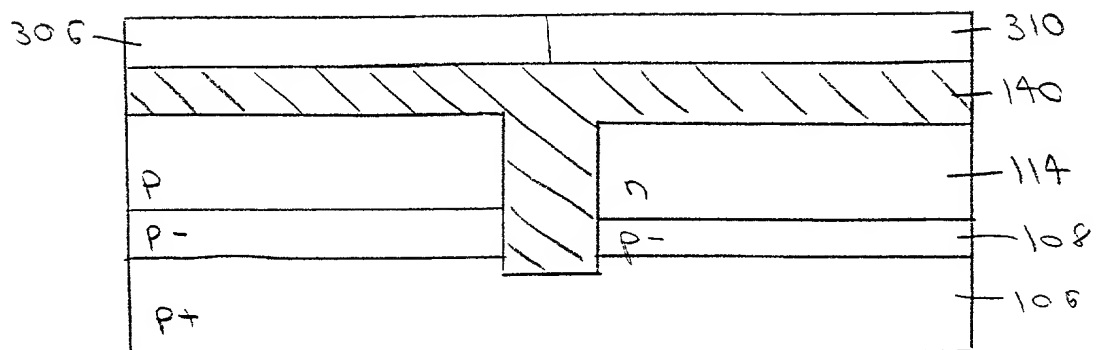


Figure 40